REMARKS

Rejection of claims 1-11 under 35 U.S.C. §103(a)

The Examiner rejected claims 1-11 under 35 U.S.C. §103(a) as being unpatentable over the combination of Chastain and Brenner. Applicant traverses the Examiner's finding of obviousness and believes the cited art, singularly or in combination does not teach or suggest the claimed invention herein.

Claim 1

Chastain teaches a computer system that comprises a plurality of processors that can process one or more threads. Brenner teaches load balancing in a computer system with a plurality of processors. In Brenner, the mutithread system is a software multithread system, meaning the support for multithreading is done with software using software supported queues. The hardware multithread system claimed herein does not have run queues as described in Brenner. Brenner combined with Chastain does not teach or suggest to determine a processor is idle when the processor is able to accept a new thread for each processor hardware thread. Since Brenner and Chastain do not teach or suggest to determine which processor can accept an additional thread in a hardware multithread or to determine which processor is idle by determining the processor can accept a new thread for each hardware thread in the processor, Applicant respectfully requests reconsideration of the rejection of claim 1 under 35 U.S.C. §103(a).

Claim 2

Claim 2 depends on claim 1, which is allowable for the reasons given above. As a result, claim 2 is allowable as depending on allowable independent claims.

Claim 3

Claim 3 depends on claim 1, which is allowable for the reasons given above. As a result, claim 3 is allowable as depending on allowable independent claims. Further, with regards to the rejection of claim 3, the Examiner states that Brenner discloses the limitation of "the thread dispatch mechanism waits for one of the plurality of processors to complete processing" recited in claim 1, citing Brenner at col. 5 lines 37-45, and col. 10 lines 49-65. Applicant has not found this teaching in the referenced portions, or any other portion of Brenner. In Brenner, a thread is assigned to an idle thread or the "lightest loaded run queue" (col. 10, line 41). There is no discussion in Brenner concerning waiting for a processor to become a processor that can accept a thread. Since Brenner and Chastain do not teach or suggest to wait until a processor can accept an additional thread, Applicant respectfully requests reconsideration of the rejection of claim 3 under 35 U.S.C. §103(a).

Claims 4-11

Claim 4 and 7 contain similar limitations to those described above with reference to claim 1. Therefore claims 4 and 7 are also allowable over the cited art. Further, claims 5-6 and 8-11 depend on claims 4 and 7 respectively, which are allowable for the reasons given above. As a result, claims 5-6 and 8-11 are allowable as depending on allowable independent claims.

Claims 12-14 have been added herein. Basis for the newly added claims is found on page 15, lines 7-8. No new matter has been added. The cited art does not teach or suggest to make all processors busy before dispatching a second thread to any processor. This allows greater processor utilization where the processors are made busy with a first thread despite any processor affinity of the threads. Considerations of these newly added claims is respectfully requested.

Conclusion

In summary, none of the cited prior art, either alone or in combination, teach, support, or suggest the unique combination of features in applicant's claims presently on file. Therefore, applicant respectfully asserts that all of applicant's claims are allowable. Such allowance at an early date is respectfully requested. The Examiner is invited to telephone the undersigned if this would in any way advance the prosecution of this case.

Respectfully submitted,

By _____
Bret J. Petersen
Reg. No. 37,417

MARTIN & ASSOCIATES, L.L.C.
P.O. Box 548
Carthage, MO 64836-0548
(417) 358-4700